Master/Bachelor Thesis

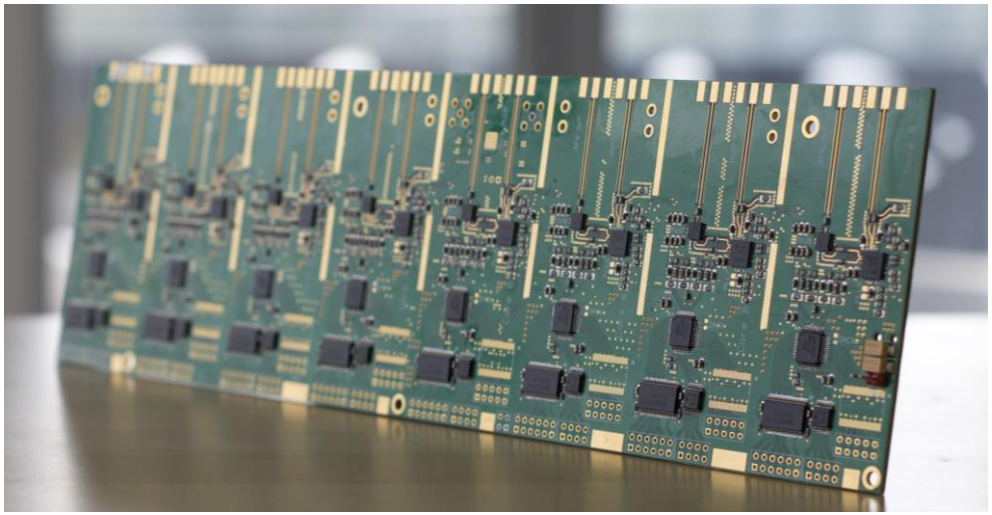
Höchstfrequenz elektronik | RWTH AACHEN UNIVERSITY

High Resolution Time-Sensing for Wideband-Transmitter Optimization

Background

At the Chair of High Frequency Electronics, a new transmitter type is being implemented. This transmitter utilizes parallelization of an analogue inverse Fourier transformation by means of multiple RF-DAC channels. Therefore, a set of synchronous transmission units must be available to provide a wideband output signal.

Carrier synchronization is a central aspect for this high-performance architecture. As current methods require high amounts of energy as well as design effort, new approaches are to be developed based on sub-picosecond time sensing circuits.



Tasks

The first task is to fully understand the transmitter architecture as well as the concept of carrier synchronisation. Furthermore, the real-time measurements by means of a time-to-digital converter (TDC) are to be investigated.

- Based on predefined boundary conditions for carrier frequency and phase resolution, necessary dynamic ranges and time resolutions must be derived.
- A sensing architecture for the given boundary conditions should be developed and validated with the help of an existing system model.
- The developed structure is to be modeled and simulated in the form of an integrated circuit with Cadence Virtuoso.
- Depending on the progress of the work, a layout of the circuit will be designed for further validation.

Contact

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