

Investigation and Design of a Two-Point Modulated Digital PLL

Background

The phase modulator is one key component of highly efficient polar transmitters, which are used in a variety of modern communication SoCs.

The phase modulator might be realized by a two-point modulated PLL, which is favorable regarding noise and linearity.

The two-point modulation requires the loop behaviour to be characterized and calibrated quite well, which is difficult for highly analog PLLs.

Therefore, digital PLL based phase modulators are investigated in this thesis.

Tasks

Your task will be to investigate, model and partially implement a modulated digital PLL.

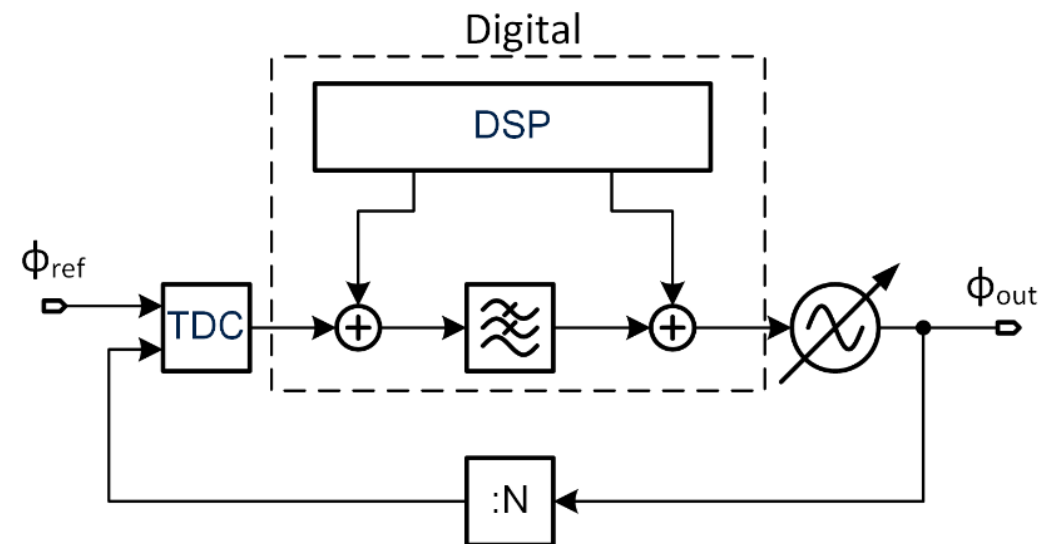
You will model the PLL in Verilog while accounting for all major nonideal effects.

From the model you will derive subblock specifications and finally implement chosen critical blocks in schematic and layout in a 65 nm CMOS technology.

You will learn about mixed-signal and digital IC design, signal processing and transmitter architectures. Additionally, you will get hands-on experience with state-of-the-art simulation tools.

The task can be broken down as follows:

- Literature study
- Verilog modeling
- Schematic/Layout design of critical blocks
- Documentation



Contact

Stefan Müller

Kopernikusstraße 16, 52074 Aachen

ICT cubes, 5th Floor, Room 538

+49 241 80 24643

stefan.mueller@hfe.rwth-aachen.de

www.hfe.rwth-aachen.de