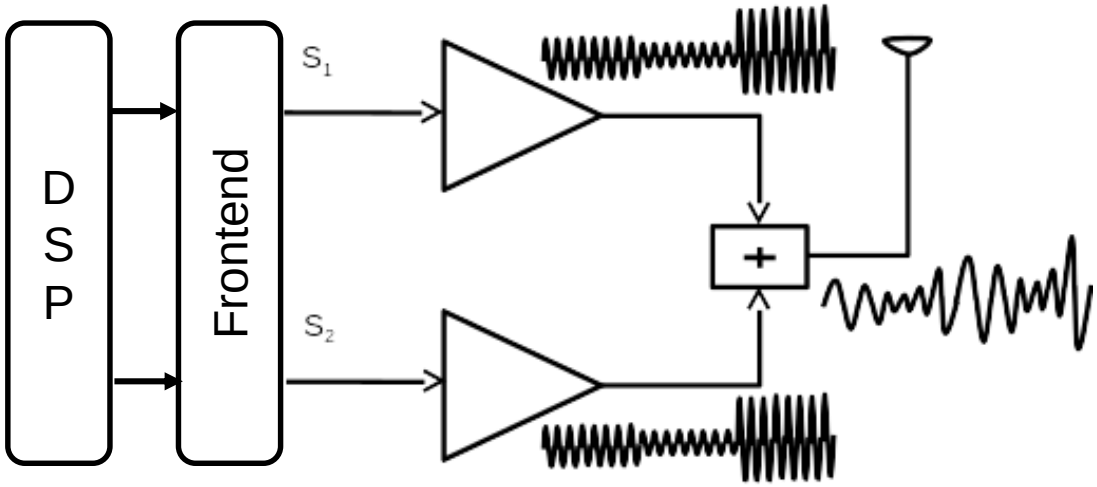
Master Thesis

Höchstfrequenz elektronik | RWTH AACHEN UNIVERSITY

Integrated DSP for a highly efficient CMOS Transmitter

Background

Modern mobile communication standards utilize modulation formats with a high peak-to-average power ratio (PAPR) which require to operate the power amplifiers (PA) deeply in their backoff region. This leads to poor energy efficiency of the whole transmitter. Therefore, we are working on architectures which break this tradeoff. A possible solution is the multilevel LINC concept, which utilizes two PAs with phase modulated inputs and switchable supply.



Tasks

Your task will be to investigate and implement a digital signal processor (DSP) in Verilog/VHDL. The DSP should generate the required signals for the multilevel LINC transmitter out of ordinary IQ-data. The difficulty is to realize the necessary nonlinear operations, while enabling high speed and low area consumption.
You will synthesise and place-and-route the DSP in a 65nm CMOS technology or on an FPGA. You will learn about digital IC design, signal processing and transmitter architectures. Additionally, you will get hands-on experience with state-of-the-art simulation tools.

The task can be broken down as follows:

- Literature study
- HDL design (Verilog/VHDL)
- Physical Design (Synthesis/PnR)
- Documentation

Contact

Stefan Müller
Kopernikusstraße 16, 52074 Aachen
ICT cubes, 5th Floor, Room 538
+49 241 80 24643
stefan.mueller@hfe.rwth-aachen.de
www.hfe.rwth-aachen.de