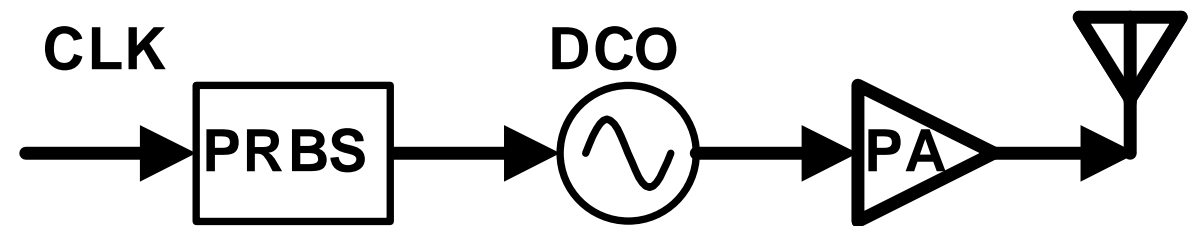


Design of high-speed clock buffer up to 24 GHz

Background

The pseudo-random bit sequence generator is applied to produce random data signals for testing all kinds of high-speed digital or mixed-signal components and system.

For high speed PRBS generator, it requires to a clock buffer to drive the logic such as DFF.



Tasks

The students task is the design of a high speed clock buffer in 65 nm CMOS:

- Literature research on clock buffer, inductive peaking method and CML structure.
- Design of the clock buffer up to 24 GHz
- Performance evaluation based on simulation results.
- Combine with PRBS generator developed at HFE

Contact

Yanlu Wang
Kopernikusstraße 16, 52074 Aachen
ICT cubes, 5th Floor, Room 538
Tel. 0241-80-24643
yanlu.wang@hfe.rwth-aachen.de
www.hfe.rwth-aachen.de