Master Thesis

Höchstfrequenz elektronik

RWTH AACHEN UNIVERSITY

Design of a 17-20 GHz Doherty PA in III-IV semiconductor technology for multibeam satellites

Background

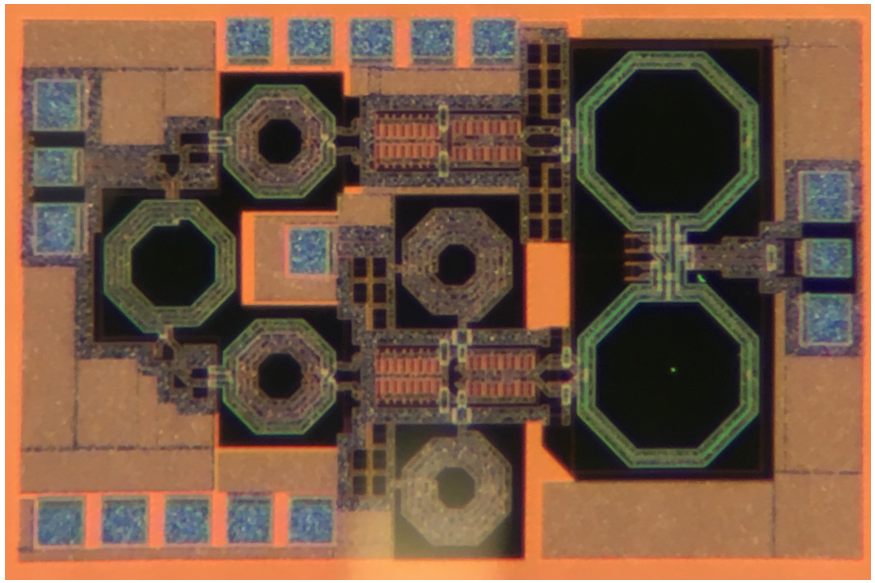
The overall radio transmitter efficiency depends on the power amplifiers performance. For common power amplifiers, the highest efficiency is reached at maximum output power. This highly decreases the efficiency of higher order modulated signals like with OFDM, which has a PAPR of at least 10dB. To achieve higher efficiencies with complex modulated signals a lot of research was done on polar transmitters, supply modulation, or PWM modulation. All of them get impractical if the modulation bandwidth gets larger than several MHz. Up to now, the Doherty Amplifier, an invention from the 1930s, is still the state of the art power amplifier for highly efficient transmitters with complex modulated signals. Load modulation can handle much higher modulation bandwidths, as it takes place in the analogue region. At HFE a new type of Doherty PA with additive-voltage supported load modulation was developed, suitable for integrated technologies. A first prototype in CMOS shows promising results in terms of bandwidth, backoff efficiency and power capability. To investigate its full potential, a mmW design has to be investigated.

Tasks

The students task is the design of a voltage combined Doherty power amplifier for 17-20 GHz in III-IV semiconductor technology based on the new approach developed at HFE:

- Literature survey on multibeam, beam steering, MIMO for satellites
- Design of Doherty PA
- Performance evaluation based on simulation results

The student will get experience in working with industrial simulation tools like ADS and Cadence. Furthermore, he/she will gain insight in high frequency circuit design.



Die-microphotograph of CMOS prototype

Contact

Eduard Heidebrecht
Kopernikusstraße 16, 52074 Aachen
ICT cubes, 5th Floor, Room 540
+49 241 80 24645
eduard.heidebrecht@hfe.rwth-aachen.de
www.hfe.rwth-aachen.de