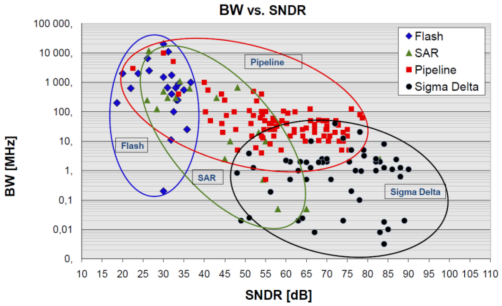
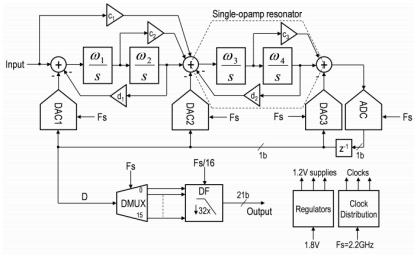
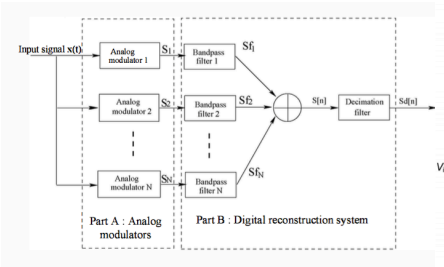
Master Thesis

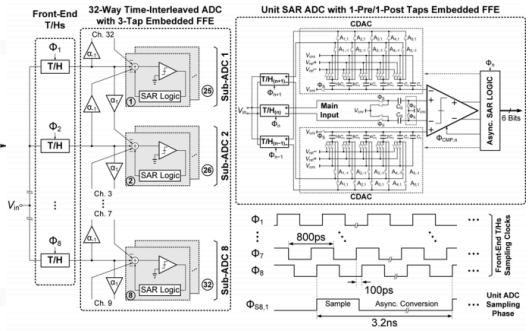
Höchstfrequenz elektronik | RWTH AACHEN UNIVERSITY

Integrated, wideband ADC for 5G on 65nm CMOS









Background

The increasing demand on integrated high data rate communication standards is pushing for high linearity / high sampling rate / wide bandwidth circuits. High speed / High resolution data converters (ADC's and DAC's) are crucial blocks to build such communication systems.
The main challenge in this topic is to design a state-of-the-art 12 bits ADC with 5GHz sampling frequency and 1 GHz bandwidth in a 65nm standard CMOS technology with competitive power consumption. Many approaches are used to realize such ADC either by combining different topologies or by using cascading of certain topology.

Tasks (The tasks can be divided into three main milestones)

- Literature survey and topology selection (8 weeks)
  - Comparison between the different topologies
  - Make a 1st design review (architecture review)
- Design (8 weeks)
  - Behavioural modelling for the building blocks of the ADC
  - Noise and power budgets allocation
  - Transistor-level design and simulations
  - Chip area estimation
  - Make a 2nd design review (design review)
- Verifications and documentation (8 weeks)
  - Layout and post layout simulations
  - Performance verification
  - Make a final design review
  - Documentation (thesis & publication)

Contact

Mohamed Elasyed
Kopernikusstraße 16, 52074 Aachen
ICT cubes, 5th Floor, Room 542
+49 241 80 24648
mohamed.elsayed@hfe.rwth-aachen.de
www.hfe.rwth-aachen.de