

Modelling of jitter transfer characteristics of All-Digital Delay Locked Loop (ADDLL)

Background

As the technological development in semiconductor technology increases rapidly, microprocessors become more and more complicated. Therefore, keeping them in optimal operating conditions and preventing any malfunction also becomes more challenging. One of the biggest challenge in the design is the high speed clock signal distribution. Since all blocks in the chip are driven by the same clock signal, internal clock generated by the local oscillator has to be very precise for all parts of the chip to avoid synchronization problems. If there is a delay mismatch between the parts, they can miss their correct state, which may lead to a significant degradation in overall performance. This clock-skew problem becomes more severe for circuits operating at high operating frequencies. Delay Locked Loops (DLLs) can be used to eliminate the clock-skew problem since they do not accumulate phase noise and timing uncertainty over multiple oscillation cycles as it gets a clean reference frequency for each clock cycle

Tasks

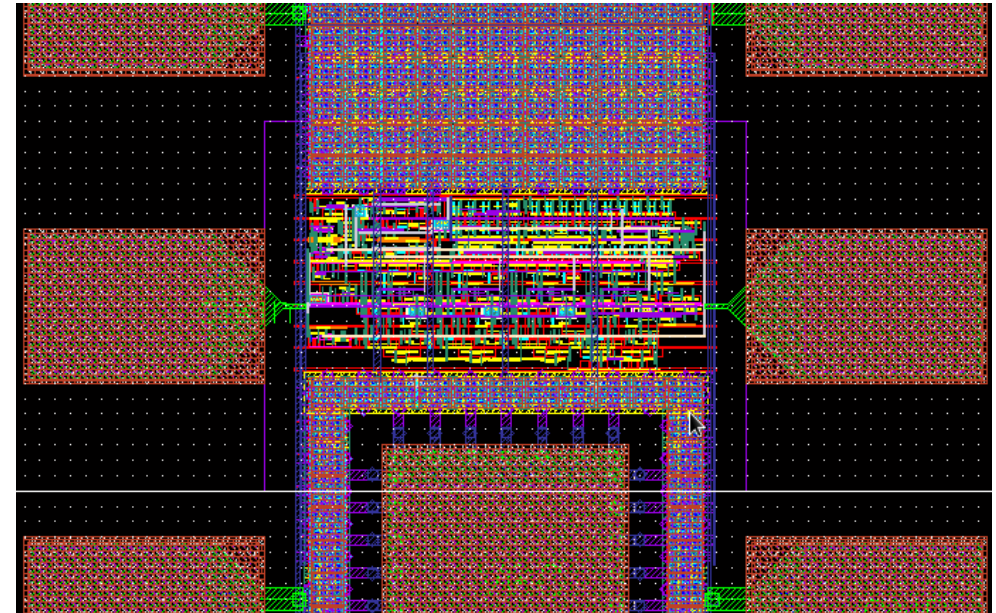
The tasks are divided into two parts:

1. Literature Research

- Understanding jitter characteristics and nature of ADDLL (cyclic jitter, peak-to-peak jitter etc.)
- Construction of mathematical analysis of jitter transfer characteristics of ADDLL.

2. Implementation

- System level design to model constructed mathematical analysis (Matlab)
- Evaluate the jitter characteristics and compared it with simulation and measurement results (some of them already handed)
- Circuit design in Cadence design tool with UMC 130nm for additional verification



Layout of ADDLL* designed in UMC 130nm

* Published in Transactions on Circuits and Systems
I: Regular Papers

3*. Possible publication (Transaction or Conference)

Further information on this and other topics could be delivered by email, telephone or discussion.

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