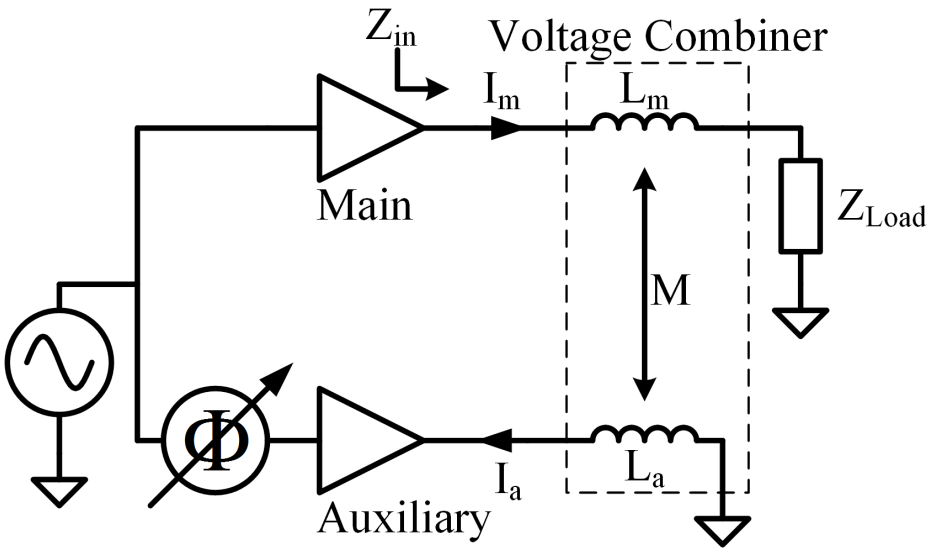
Master Thesis

Design of a 5G compliant voltage combined Doherty Power Amplifier in CMOS

Background

The overall radio transmitter efficiency depends on the power amplifiers performance. For common power amplifiers, the highest efficiency is reached at maximum output power. This highly decreases the efficiency of higher order modulated signals like with OFDM, which has a PAPR of at least 10dB. To achieve higher efficiencies with complex modulated signals a lot of research was done on polar transmitters, supply modulation, or PWM modulation. All of them get impractical if the modulation bandwidth gets larger than several MHz. Up to now, the Doherty Amplifier, an invention from the 1930s, is still the state of the art power amplifier for highly efficient transmitters with complex modulated signals and it is a promising candidate for the upcoming 5G communication standard. Its working principle is based on load modulation, which is achieved with the help of an auxiliary amplifier. Load modulation can handle much higher modulation bandwidths, as it takes place in the analogue region. At HFE a new type of voltage combined Doherty Amplifier was developed, suitable for CMOS and MMIC integration to reach higher frequencies.



Tasks

The students task is the design of a voltage combined Doherty power amplifier in CMOS 130nm based on the new approach developed at HFE:

- Literature survey on 5G systems at lower frequency bands
- Design of 5G CMOS PA assigned for lower frequency band (3-5GHz)
- Performance evaluation based on simulation results
- If time is left: Performance evaluation with modulated signals

The student will get experience in working with industrial simulation tools like ADS and Cadence. Furthermore, he/she will gain insight in high frequency circuit design.

Contact

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