Bachelor/Master Thesis
Multiplying Delay-Locked Loops (MDLL) (Injection Locking PLL)

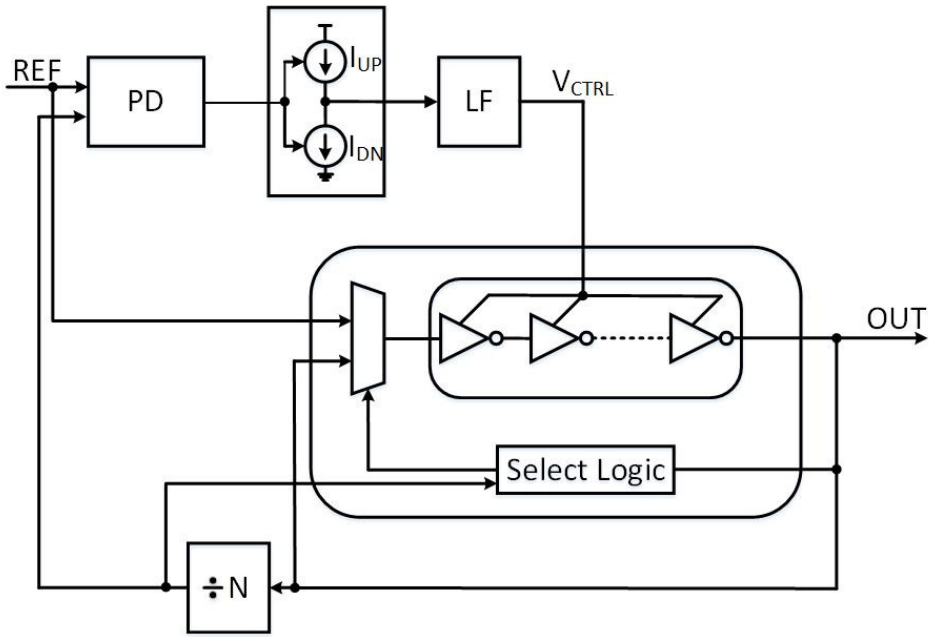
Background:

As the technological development in semiconductor technology increases rapidly, microprocessors become more and more complicated so this will lead a bigger chip size since more Integrated Circuits (IC) blocks are integrated into the same chip and higher operating frequency that enables high speed operations. Thus, PLL is one of the most important block in the system to generate clock frequency. However it has drawbacks in terms of phase noise and jitter performance due to the bandwidth trade-off in its design. Since phase noise of phase detector is low-pass filtered while oscillator phase noise is high-pass filtered, bandwidth selection is extremely critical to get good phase noise performance with low power consumption and small chip area. Multiplying Delay-Locked Loops (MDLL) is proposed to overcome these difficulties by replacing every Nth edge of a running ring oscillator with a reference frequency for each N cycle. This allows significant jitter degradation without power consumption and are penalty.

Tasks:

The tasks are divided into two parts:

1. Literature Research
   - Searching suitable MDLL topologies for clock multiplication
   - Matlab modelling for the complete system (defining parameters of the system)
2. Implementation
   - Circuit design in Cadence with TSMC 65nm technology
   - Layout of critical blocks (possible tapeout)
   - Post layout simulations (Verification)



Conventional block diagram of MDLL

Further information on this and other topics could be delivered by email, telephone or discussion.

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