Zero-bias, 50 dB Dynamic Range, Linear-in-dB V-band Power Detector based on CVD Graphene diode on Glass

Mohamed Saeed, Student Member, IEEE, Ahmed Hamed, Student Member, IEEE, Zhenxing Wang, Mehrdad Shaygan, Daniel Neumaier, and Renato Negra, Member, IEEE

Abstract—In this paper we report the design, fabrication, and demonstration of a compact, V-band, zero-bias, linear-in-dB power detector based on our in-house metal-insulator-graphene (MIG) diode fabricated on glass substrate. The presented circuit is optimized for the frequency band 40 – 75 GHz. The measured prototype shows a repeatable measured dynamic range of at least 50 dB with down to −50 dBm sensitivity on 500 μm thick quartz substrate. It also shows input return loss better than −9.5 dB over the entire design bandwidth. The measured tangential responsivity for the fabricated circuit on glass is 168 V/W at 2.5 GHz and 15 V/W at 60 GHz. The obtained results together with the robust device fabrication based on chemical vapor deposition (CVD) graphene promote the proposed scheme and device for repeatable, statistically stable millimeter-wave and submillimeter-wave applications.

Index Terms—Chemical Vapor Deposition (CVD), Diode, Graphene, Power Detector, Linear-in-dB.

I. INTRODUCTION

GRAPHENE is a 2D material with outstanding electrical and mechanical properties. The reported carrier electron mobility and saturation velocity [1], together with the ability to large-scale integration on different substrates make graphene a perfect candidate for RF, millimeter-wave, and submillimeter-wave circuit applications such as Internet of Things (IoT), Near Field Communications (NFC), Radio Frequency Identification Device (RFID) tags, flexible electronics, smart wearables, medical, and communications applications.

Graphene-based devices and circuits are under continuous development [2] to make use of these unique properties. Reported graphene field effect transistor (GFET) based circuits [3]-[5] suffer from lower cutoff frequency ($f_T$) and lower maximum oscillation frequency ($f_{max}$) than what could be expected based on the high carrier transport properties wherein graphene-metal contact resistance plays a deleterious role [6]. In addition, the poor current saturation of single-layer GFETs causes low dc gain. On the other hand, exfoliated GFETs reported good high frequency characteristics [7], but suffer from reproducibility and scalability. The chemical vapor deposition (CVD) method in producing large-scale graphene has the advantage of reproducibility which is crucial for device modeling enabling the usage of graphene circuits in different commercial applications. Many studies have been carried out to produce CVD graphene with improved mobility to be used in stable and large-scale production processes [8].

Power detectors are one of the direct applications for exploring the high carrier mobility in graphene. Power detectors are crucial elements in wireless communication systems. Many applications such as radio-frequency identification (RFID), automatic gain control (AGC), and energy harvesting require sensitive, low-voltage drop, and low capacitance power detectors. The linear-in-dB detector is one type of power detectors that is used mostly to measure accurately the power of high peak-to-average ratios RF signals [9]. This technique is used in transmitters to control the output power levels of the power amplifier (PA) and in receivers to indicate the RF signal strength in order to adjust the gain of the receiver to ensure a constant signal strength at the input of the analog-to-digital converter (ADC). Employing GFETs as linear power detector devices has been reported in [10]-[12]. The demonstrated GFET power detectors are leveraging the nonlinear channel resistance property above the FET extrinsic $f_T$ and $f_{max}$ limitations. The 3-dB detection bandwidth of GFET detectors is given by $1/(2\pi C_1 R_t)$ where $C_1$ is the total gate capacitance which consists of gate-to-source capacitance, $C_{gs}$, and gate-to-drain capacitance, $C_{gd}$. While $R_t$ is the total resistance and is formed by the gate resistance, $R_g$, in series with the source resistance, $R_s$. Using GFETs as power detectors has two main limitations. The first limitation comes from the excess capacitance of $C_{gs}$, which limits the 3-dB detection bandwidth of the power detector. The second one is the limited dynamic range related to the small-signal dependency of the nonlinear channel resistance. In addition, the substrate plays a key role in the achievable sensitivity. Detectors fabricated on expensive millimeter-wave 100 μm SiC with relative permittivity ($\epsilon_r$) equals 9 in [10] and [12] provide higher sensitivity compared to the work in [11] which was fabricated on 500 μm glass substrate with $\epsilon_r$ equals 4, due to higher losses at high frequencies for microstrip transmission line-based design.

In this work we extend the work reported in [13], showing more details about the operation and characterization of the MIG diode, input impedance measurements, and the extracted model. In addition, we report more details about the operation of the proposed detector circuit and input impedance matching network design.
Recently, metal-insulator-metal (MIM) diodes have attracted a lot of attention due to two main advantages over semiconductor based pn-diodes and Schottky-diodes. First, the low diode series resistance which leads to improved performance in higher frequency applications. In addition, these diodes can be fabricated in a thin-film process which makes them attractive for nonsemiconductor based systems like glass and alumina or flexible substrates [14]-[16]. However, the performance of MIM diodes in terms of asymmetry and nonlinearity are inferior in performance compared to other semiconductor based diodes.

A. Diode operation and fabrication

Replacing one metal electrode by an exfoliated graphene has been reported in [17] demonstrating higher nonlinearity and asymmetry compared to state-of-the-art MIM diodes.

Fig. 1(a) compares the principal structures of MIM and MIG diodes. The diode operation is described by the thermal emission theory. As shown in Fig. 1(b), in the reverse bias, the barrier height for electrons to transfer from M1 to M2 in the MIM, and from M to G in the MIG decreases with increasing reverse voltage until it reaches the potential difference between the work function of M1 and the conduction band edge of the insulator for MIM. In the MIG case, the barrier decreases until it reaches the potential difference between the work function of M and the conduction band edge of the insulator. In forward bias, the barrier height for electrons to transfer from M2 to M1 in MIM is reduced until it reaches the potential difference between the work function of M2 and the conduction band edge of the insulator. This creates the necessary asymmetry between forward and reverse operation. In the case of MIG diode, the barrier height for electrons to transfer from G to M decreases with the increasing forward bias, i.e. the bias induced barrier lowering, which explains the high on-current, higher asymmetry for the MIG compared to the MIM diode.

Another improvement in our CVD MIG diode is achieved by embedding the metal electrode into the substrate to minimize the parasitic capacitance and therefore, improve the frequency characteristics of the diode.

The MIG diodes are fabricated on 500 µm glass substrate as shown in Fig. 2. The entire fabrication process was performed using optical contact lithography. First 200 nm deep trenches were etched into the substrate by reactive ion etching (RIE) for the deposition of embedded metal electrodes. With the same resist mask after etching, the trenches were then filled with a stack of 180 nm Al and 20 nm Ti using e-beam evaporation, followed by lift-off. Then, a layer of 6 nm TiO₂ is deposited by atomic layer deposition (ALD) at 300 °C using an oxygen plasma process with titanium tetrachloride (TiCl₄) as precursor. Vias through the TiO₂ layer were opened before TiO₂ deposition.
by Ar sputtering, and then sealed with 20 nm Ni without breaking the vacuum. CVD grown graphene is transferred onto the sample using polymethyl-methacrylate (PMMA) as a supporting layer. After patterning the graphene by oxygen plasma, metal contacts to the graphene were fabricated by sputter deposition and lift-off, with 20 nm Ni and 100 nm Al on top. The chip micrograph of the fabricated MIG is shown in Fig. 3 occupying overall active area of 160 $\mu$m$^2$ with two fingers.

The atomic force microscope (AFM) image of the embedded electrode before TiO$_2$ deposition is shown in Fig. 4. The root mean square (RMS) roughness of the electrode surface is 6.0 nm, based on the height distribution from the middle part of the shown AFM image. Due to the excellent surface coverage of the atomic layer deposition (ALD) technology, the TiO$_2$ barrier layer can be formed properly onto the embedded electrode, which is crucial for the performance of the diode.

B. Diode characterization

On wafer, dc characterization of the fabricated devices is shown in Fig. 5 demonstrating a high on-current density of 176 A/cm$^2$. From the measured I-V characteristics we can calculate the diode figure-of-merits FOMs according to [18]

$$f_{\text{Asym}} = \frac{|J_F|}{J_R},$$

$$f_{\text{NL}} = \frac{dJ}{dV} / J,$$  

and

$$f_{\text{RES}} = \frac{d^2J}{dV^2} / \frac{dJ}{dV},$$

where $J_F$ and $J_R$ are the forward and reverse current densities, respectively, while $J$ is the current density of the diode.

Calculating the FOMs of our diodes show high asymmetry up to 525, with a strong maximum nonlinearity of up to 10, and responsivity of up to 27 A/W. These features especially for the responsivity, outperform state-of-the-art MIM and schottky diodes [19] and [20]. A comprehensive discussion regarding the device physics, fabrication stability statistics for 11 samples, and comparison with state-of-the-art MIM diodes is reported by the authors in [20].

In addition to the dc characterization, S-parameter measurements are carried out with a network analyzer and on-wafer Cascade GSG-100 probes. The used calibration is the SOLT method using Cascade CSR-8 standard substrate in the frequency range 1 – 70 GHz at power level of $-30$ dBm as shown in Fig. 6. From the measurements on various fabricated MIG diodes the impedances are extracted to be used in the design of the input matching circuit of the power detector.

The extracted S-parameters up to 70 GHz are used to extract the MIG diode equivalent circuit shown in Fig. 7, where $R_s$ is the linear series resistance of the metal interconnects combined with Graphene-Metal contact resistance, $R_j$ is the nonlinear junction resistance, and $C_j$ is the nonlinear capacitance of the junction diode, $C_g$ is the linear geometric parasitic series capacitance between the embedded electrode and the graphene. The physical design of the diode should be such that the geometric capacitance is larger than the nonlinear junction capacitance. $C_f$ is the parasitic fringing capacitance between the two metal electrodes. Thanks to the substrate...
TABLE I
PASSIVE COMPONENTS VALUES OF THE EXTRACTED MODEL AT ZERO BIAS

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_p$</td>
<td>PAD parasitic capacitance</td>
<td>8</td>
<td>fF</td>
</tr>
<tr>
<td>$R_s$</td>
<td>PAD and interconnects parasitic resistance</td>
<td>17</td>
<td>Ω</td>
</tr>
<tr>
<td>$L_s$</td>
<td>PAD and interconnects parasitic inductance</td>
<td>40</td>
<td>pH</td>
</tr>
<tr>
<td>$C_{f-pad}$</td>
<td>PADs Fringing capacitance</td>
<td>10</td>
<td>fF</td>
</tr>
<tr>
<td>$C_{f}$</td>
<td>Anode and cathode fringing capacitance</td>
<td>2.5</td>
<td>fF</td>
</tr>
<tr>
<td>$C_g$</td>
<td>Linear geometrical capacitance</td>
<td>0.4</td>
<td>pF</td>
</tr>
<tr>
<td>$C_j$</td>
<td>Junction nonlinear capacitance</td>
<td>51</td>
<td>fF</td>
</tr>
<tr>
<td>$R_j$</td>
<td>Junction nonlinear resistance</td>
<td>30</td>
<td>Ω</td>
</tr>
</tbody>
</table>

embedded electrode the value of this capacitance is negligible. $L_s$ is the series parasitic PADS and interconnects inductance, $C_{f-pad}$ is the fringing capacitance between the two probing PADS, $C_p$ is the PAD parasitic capacitance. Extracted values at zero bias are listed in Table I. The extracted model is used in the design of the proposed detector.

### III. POWER DETECTOR CIRCUIT

#### A. Circuit design

The proposed schematic including the MIG diodes is shown in Fig. 8. The power detector core consists of the three MIG diodes D₁, D₂, and D₃. D₂ is the main half-wave rectifier (HWR) diode, and together with the clamp diode D₁ form one stage Cockcroft-Walton voltage doubler circuit [21] to improve the sensitivity of the power detector.

The extended dynamic range is achieved by combining the square-law detector operation with high sensitivity, together with the logarithmic detector operation which has excellent dynamic range. At low input power levels, $P_{in}$, the clamp diode D₁ acts as a capacitor, while the HWR operation is done by D₂ which operates in the square-law region, producing a current proportional to $P_{in}$ according to the Taylor expansion of the diode I-V characteristics assuming a sinusoidal input signal as follow:

$$i_{D_2} \approx k v_p^2, k = \frac{I_o}{4\eta V_T},$$

where $v_p$ is the peak voltage of the input signal, $I_o$ is the saturation current, $\eta$ is the diode ideality factor, and $V_T$ is the thermal voltage.

On the other hand, the input RF power $P_{in}$ is related to the input peak voltage, $v_p$, according to the relation:

$$P_{in} = \frac{v_p^2}{2R_{in}},$$

which leads to the proportionality of $i_{D_2}$ to $P_{in}$.

At high input powers, the nonlinearity of the shunt diode D₁ is added to the nonlinearity of D₂ resulting in higher compression and extended square-law region for the rectifier circuit. The MIG diode extracted model is used to simulate a HWR circuit formed by the diode D₂ with a resistive load, and the proposed combination of D₁ and D₂ with a resistive load. Simulation results shown in Fig. 9 demonstrate the pronounced extension of the square-law region of the proposed detector.

Diode D₃ as a load is responsible to produce an output dc voltage which is proportional to the logarithmic of the current. Since the current is proportional to the input RF power $P_{in}$, as shown above, the output voltage is proportional to the logarithmic power at the input.

Since the proposed detector is zero-bias and owing to the properties of the MIG diode, there is no need for an extra dc

Fig. 8. Graphene power detector schematic based on MIG diode.

Fig. 9. Simulated responsivity of the HWR diode and the proposed scheme compared to the square-law detection.

Fig. 10. Simulated core detector circuit input impedance $S$-parameters for proper input matching design from 40 – 70 GHz.
bias pad. Other advantages of zero-biasing are reduced noise generated by the ON-current of the diodes and low power operation.

B. Input matching

Impedance matching at the input of power detector is essential to achieve maximum power transfer and to avoid antenna back radiation. Using the measured $S$-parameters of the MIG diode, we simulate the core detector circuit as shown in Fig. 10, determining the input impedance at the midband frequency of 55 GHz and match it to 50 Ω. The input matching network, as shown in Fig. 11, is realized combining resistive and reactive passive components to ensure wide bandwidth and low sensitivity to process tolerances.

IV. Measurement Results

The fabricated power detector circuit as shown in Fig. 12 occupying 0.15 mm$^2$ of chip area including pads. The design is repeated on multiple chips to ensure a statistically stable performance of our Back-End-Of-Line (BEOL) and CVD-graphene process. To characterize the fabricated detector a Keysight® PNA-X network analyzer is used to measure the $S$-parameters, as well as a calibrated power source to determine the circuit sensitivity and dynamic range. A Keysight® N8488A power sensor and a Keysight® E4418B power meter are employed in the power calibration of the source.

$S$-parameter measurement results for the fabricated circuits are shown in Fig. 13. The measured input return loss is better than −10 dB for the entire band from 40 – 70 GHz for almost all measured samples. Repeatability of the fabricated circuits

![Fig. 11. Equivalent input matching circuit schematic.](image1)

![Fig. 12. Chip micrographs of the fabricated power detector circuit on 500 μm quartz substrate occupying 360 μm x 430 μm of chip area.](image2)

![Fig. 13. Measured and simulated $S_{11}$ for different samples in the frequency band 40 – 70 GHz.](image3)

![Fig. 14. Detector dynamic range and sensitivity measurement results at 60 GHz for different fabricated samples.](image4)

![Fig. 15. Measured tangential signal sensitivity ($TSS$) in the band 40 – 70 GHz.](image5)

![Fig. 16. Detector tangential responsivity measurement results up to 70 GHz.](image6)
is also proven by the consistency of the measurement results. Fabrication tolerances lead to a slight shift in center frequency of the matching network and higher losses compared to the Electromagnetic (EM) simulations.

Detector dynamic range and sensitivity measurements are conducted by sweeping the RF power at certain frequencies in the band and connecting the detector output to dc meter with 800 kΩ input resistance. Fig. 14 shows the measurement results for multiple samples at 60 GHz. The fabricated circuit provides at least 50 dB of dynamic range. Measurements are repeated for different samples and the advantage of CVD graphene process repeatability is demonstrated. The measured tangential signal sensitivity TSS is shown in Fig. 15, demonstrating better than −50 dBm over the entire band.

To measure the tangential responsivity in V/W for the fabricated diodes we apply −30 dBm over the frequency range from 2.5 GHz to 70 GHz and measure the output voltage with a 50 Ω load. Since we do not have good input matching for the complete frequency range from 2.5 – 70 GHz, the measured $S_{11}$ is used to calculate the incident power on the device. Measurement results are shown in Fig. 16. Responsivities as high as 15 V/W at 60 GHz, and 168 V/W at 2.5 GHz depicting outstanding responsivity at 50 Ω load.

Table II compares the presented power detector with GFET-based power detectors. All power detectors in this comparison - except for the one presented in this work - are linear detectors based on GFET. In addition, all GFET-based detectors in the comparison consist of a single device while the presented detector is based on three MIG diodes. It is clearly demonstrated that the measured dynamic range, sensitivity, responsivity, and circuit complexity in the proposed design with repeatable and reproducible results outperform other GFET-based detectors.

The Schottky diode-based detector reported in [22] achieves a responsivity of 7000 V/W because it allows to use a 500 kΩ thin film resistor as load resistance. Conversely, the reported values in Table II for the presented detector are with 50 Ω load resistance which translates to a lower responsivity. For the presented detector measurements shown in Fig. 14 with 800 kΩ load resistance, the calculated tangential responsivity at −30 dBm is 15000 V/W. In addition, the reported return loss of the Schottky detector in [22] is about 4 dB. It can be seen from (4) and (5) that increasing the load and input resistances of the detector leads to higher responsivity at the expense of reduced bandwidth of the detected signal and higher return losses respectively. Compared to the MIM diode-based detector reported in [23], the presented circuit outperforms the MIM diodes-based detector operating at 0.2 V.

Performance of MIM diode-based circuits suffers from design challenges especially regarding the oxide thickness [24] which plays a crucial role in increasing the nonlinearity and the charge transfer mechanism.

V. DISCUSSION AND CONCLUSION

The presented power detector employs a CVD MIG diode device and demonstrates the first linear-in-db detector circuit based on graphene devices. The fabricated circuit outperforms GFET based power detectors with the same substrate. The repeatability of the results is also shown owing to the robust fabrication technique based on CVD graphene. High dynamic range, high sensitivity, and diode-based design promote the potential of the circuit in millimeter-wave, and sub millimeter-wave applications.

REFERENCES


<table>
<thead>
<tr>
<th>Ref.</th>
<th>Substrate</th>
<th>Scheme</th>
<th>Dynamic Range (dB)</th>
<th>Sensitivity (dBm)</th>
<th>Responsivity (V/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[10]</td>
<td>SiC</td>
<td>GFET</td>
<td>40</td>
<td>−73</td>
<td>71 V/W at 2 GHz, and 33 V/W at 110 GHz</td>
</tr>
<tr>
<td>[12]</td>
<td>SiC</td>
<td>GFET</td>
<td>N.A</td>
<td>N.A</td>
<td>2 V/W at 96 GHz</td>
</tr>
<tr>
<td>[22]</td>
<td>$Al_2O_3$</td>
<td>GaAs Schottky diode</td>
<td>N.A</td>
<td>N.A</td>
<td>7000 V/W at 70 GHz</td>
</tr>
<tr>
<td>This work</td>
<td>Glass</td>
<td>MIG diode</td>
<td>&gt;50</td>
<td>&lt;−50</td>
<td>168 V/W at 2.5 GHz , and 15 V/W at 60 GHz</td>
</tr>
</tbody>
</table>

TABLE II

STATE-OF-THE-ART COMPARISON OF DIFFERENT POWER DETECTORS BASED ON GRAPHENE


Mohamed Saeed received the B.Sc. and M.Sc. in Electrical Engineering from Ain Shams University, Cairo, Egypt, in 2004 and 2011, respectively. From 2005 to 2013 he worked for Si-Ware Systems, Cairo, Egypt, designing ADCs/DACs for video and communications applications, also he designed many power management circuits and was in the team that developed the FTIR spectrometer solution that was announced in 2012. He built and led the layout and physical verification team in the same company. Since August 2013 he is working towards the PhD degree in the chair of High Frequency Electronics at RWTH Aachen University, Aachen, Germany. His research interests are developing microwave graphene compatible MMIC process backend. Designing, measuring and modeling graphene based RF and microwave devices and circuits.

Ahmed Hamed received the B.Sc. and M.Sc. in Electrical Engineering from Ain Shams University, Cairo, Egypt, in 2004 and 2012, respectively. From 2004 to 2011 he was an RF design engineer for SySDSoft Inc., Cairo, Egypt, and Si-Ware Systems Inc., Cairo, Egypt, designing RF circuits for Bluetooth and WIMAX transceivers as well as high frequency stability LC reference oscillators. In 2011 he joined Hitite Microwave corporation, where he worked on the design of microwave mixers, switches and power detectors for E-band communication systems using GaAs and SiGe technologies. Since December 2013 he is working towards the PhD degree at RWTH Aachen University, Aachen, Germany. His research interests include graphene MMIC process backend development and graphene-based micro- and millimeter-wave circuit design.

Zhenxing Wang received the Ph.D. degree in nanoelectronics from the Department of Electrical Engineering, Peking University, Beijing, China, in 2012. From 2012 to 2014 he worked in the University of Erlangen-Nuremberg as post doctoral researcher. He is currently with AMO GmbH in Aachen, Germany, where he is focusing on graphene based electronic devices and circuits.

Mehrdad Shaygan holds a PhD degree in the Nanotechnology/Nanoelectronics (2014) from Pohang University of Science and Technology (POSTECH), South Korea. During his PhD, he has been working on different types of nanomaterials and their potential application in nanoelectronics including field effect Transistors and Optoelectronic Devices. Currently, he is a research associate at AMO working on graphene based electronic devices.

Daniel Neumaier is the head of the Graphene group at AMO GmbH since 2009. He studied physics obtained his PhD degree in 2009. From 2006 until 2009 he worked in the group of Dieter Weiss at the University of Regensburg in the field of GaAs based spintronics. In the Flagship-Project Graphene Daniel Neumaier is leader of the work-package Electronics Devices and head of Division 3. His research interests are graphene based devices for high-frequency electronic, optoelectronic and sensor applications.

Renato Negra received the M.Sc. degree in telematics from Graz University of Technology, Graz, Austria, and the Ph.D. degree in electrical engineering from ETH Zurich, Zurich, Switzerland, from 1998 to 2000 he was with Alcatel Space Norway AS (now NorSpace AS), Horten, Norway where he was involved in the design and characterisation of space-qualified RF equipment. In 2000 he joined the Laboratory for Electromagnetic Fields and Microwave Electronics at the ETH Zurich. There, his PhD research was focused on power-efficient linear amplification of wireless communication signals. He was a Post-Doctoral Fellow at iRadio Lab, University of Calgary, Canada, working on switching-mode power amplifiers and advanced wireless transmitters from 2006 to 2008. Within the Ultra high speed Mobile Information and Communication (UMIC) Research Centre, RWTH Aachen University, Germany, he was appointed as Assistant Professor for Mixed-Signal CMOS Circuits from June 2008 till December 2013. Since December 2013 he is full Professor and is holding the Chair of High Frequency Electronics at the same university. His research interests are high frequency circuits and systems in both silicon, III-V and 2D-material technologies. Particular interests include power amplifiers and transceiver architectures.